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TITLE: Heterojunction field effect transistor

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On the other hand, in "High Efficiency Power Module Using HEMT for PDC", Preliminary Report of 1996 Institute of Electronics, Communication and Information, Electron-Science Meeting, C-422, there has been disclosed a multistage recessed InGaAS/AlGaAs HEMT, in which an etching stopper layer consisted of n.sup.- AlGaAs is provided between an n.sup.+ GaAs layer and an n.sup.- GaAs layer to perform selective etching to form the recessed structure with good controllability and reproduction ability. On the other hand, in FIG. 1 of the above-identified publication, there is disclosed a structure, in which a gate metal and a neighborhood semiconductor layer are not contacted.

In the above-identified known publication, there is no disclosure of a fabrication process of the HEMT. Thus, assuming from the structure, since the mask for forming the gate metal is formed after formation of the two stage recessed structure through at least two lithographic steps, at least three lithographic steps are necessary.

A first aspect of the field effect transistor according to the present invention comprises: a hetero junction semiconductor crystal having at least a channel layer of InGaAs or GaAs, a first AlGaAs layer. a first GaAs layer, a second AlGaAs layer and an n-type second GaAs layer; and

an ohmic electrode
contacting with said second GaAs layer and said channel layer or with said
second GaAs layer and said first AlGaAs layer doped with a donor.

A second aspect of the fabrication process of a field effect transistor
according to the present invention comprises the steps of: forming a hetero
junction semiconductor crystal having a channel layer of InGaAs or GaAs, a
first AlGaAs layer, a first GaAs layer, a second AlGaAs layer and an n-type
second GaAs layer; selectively etching said first GaAs layer with respect to
said first AlGaAs layer after said second GaAs layer and said second AlGaAs
layer are removed using a mask which has an opening at an ohmic region; forming
an ohmic electrode by deposition and lift off of ohmic metal and heat treatment
for alloying so as to contact at least said second GaAs layer and said channel
layer or said second GaAs layer and said first AlGaAs layer doped with a donor.

On the other hand, a hetero junction FET fabricated on an InP substrate,
constituted by substituting AlGaAs layer with In.sub.0.5 Al.sub.0.5 As layer
and substituting In.sub.0.2 Ga.sub.0.8 As layer with In.sub.0.5 Ga.sub.0.5 As
layer, can obtain similar effect. In this case, it may be possible to employ
tartaric acid etchant for an InP hetero junction FET in place of a dry etching
method introducing a mixture gas of chloride gas containing only chlorine and
fluoride gas containing only fluorine (e.g. BCl.sub.3 +SF.sub.6) as halogen
element, into the ECR etching device or the RIE device employed in the GaAs
type hetero junction FET.

"High Efficiency Power Module Using HEMT for PDC" Yoshida et al Preliminary
Report of 1996 Institute of Electronics, Communication

and Information;
Electronics Science Meeting, C-422; p. 80.